

Figure 1B

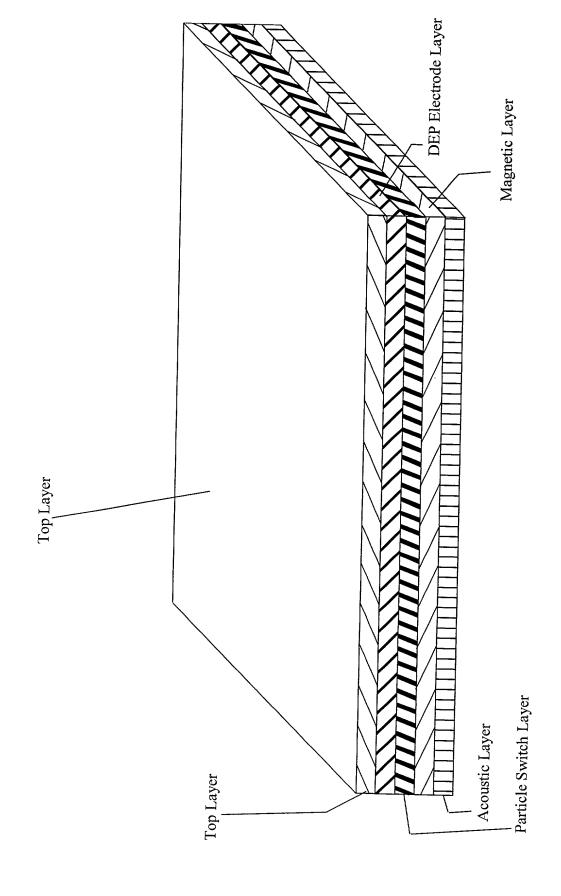


Figure 1C

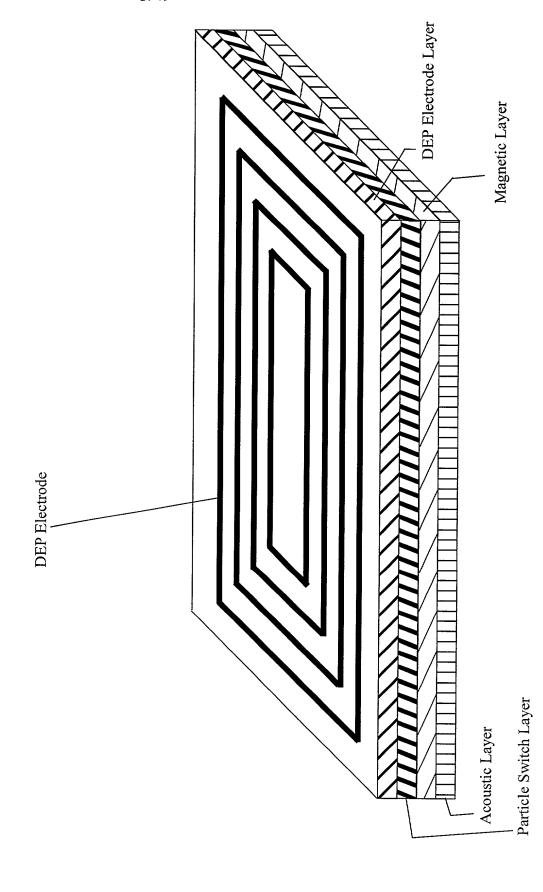


Figure 1D

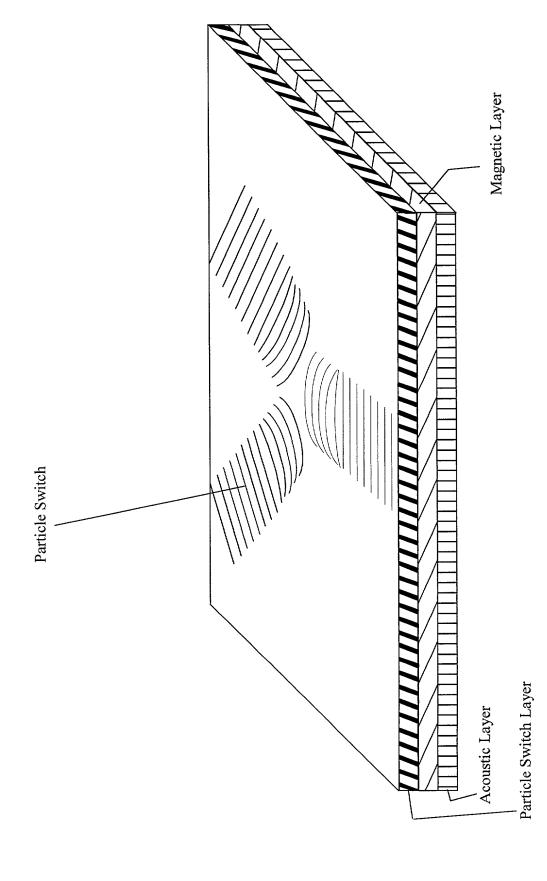


Figure 1E

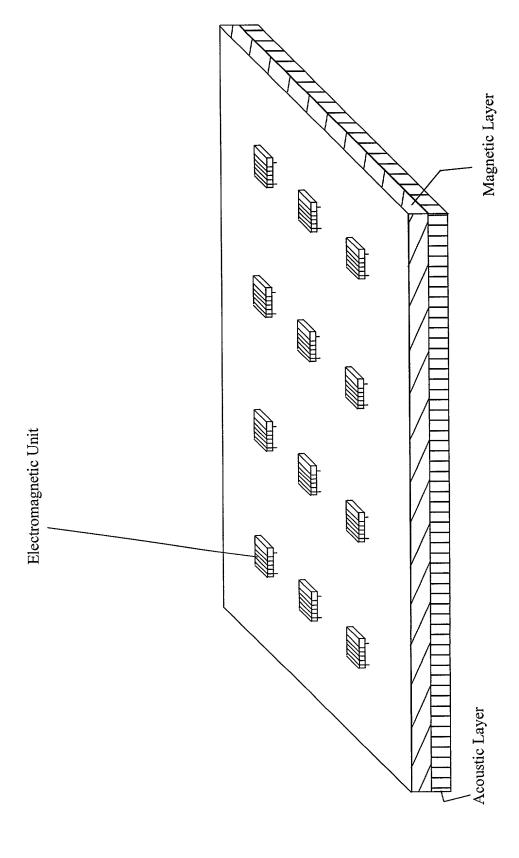
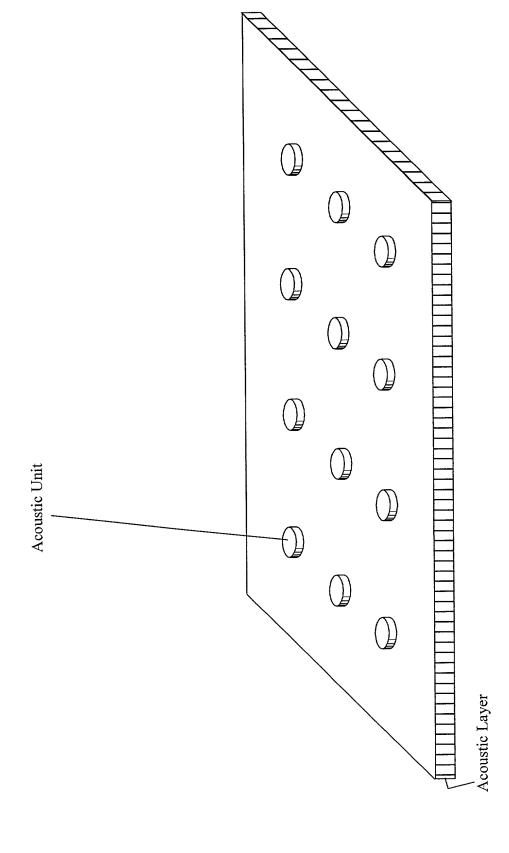


Figure 1F



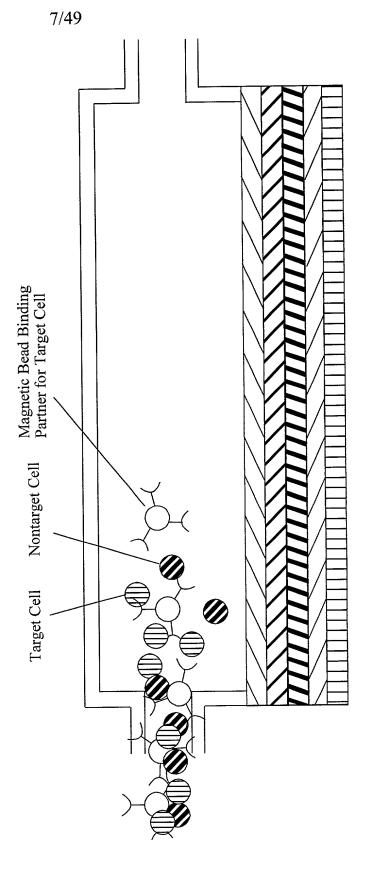


Figure 2B

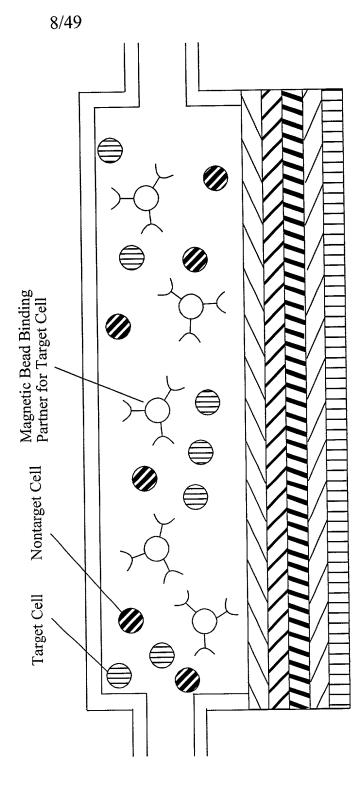


Figure 3

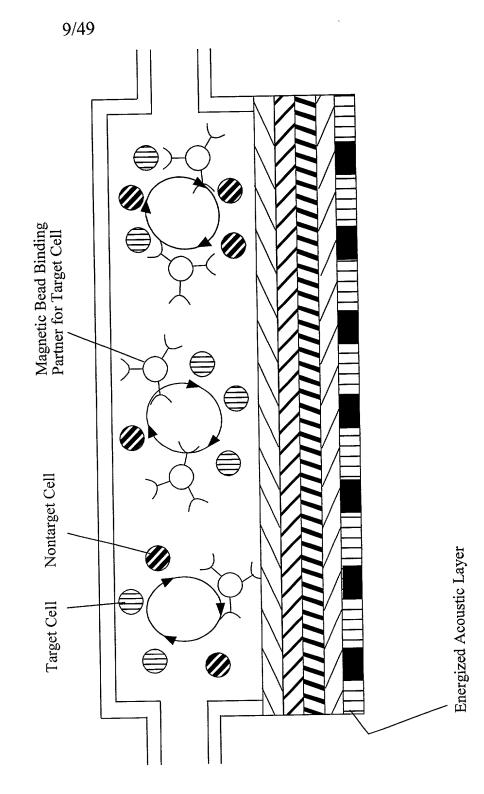


Figure 4

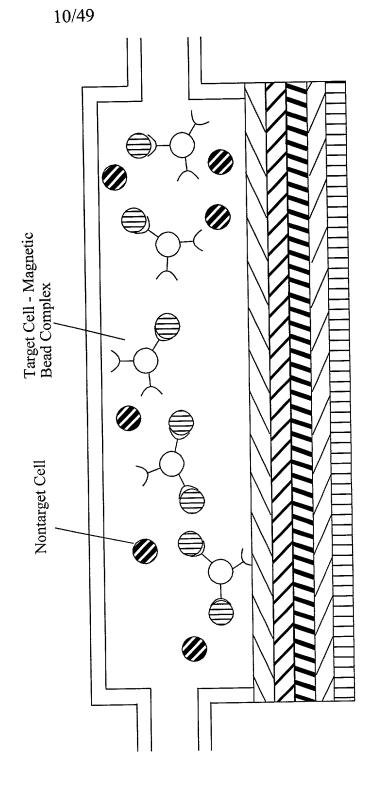


Figure 5A

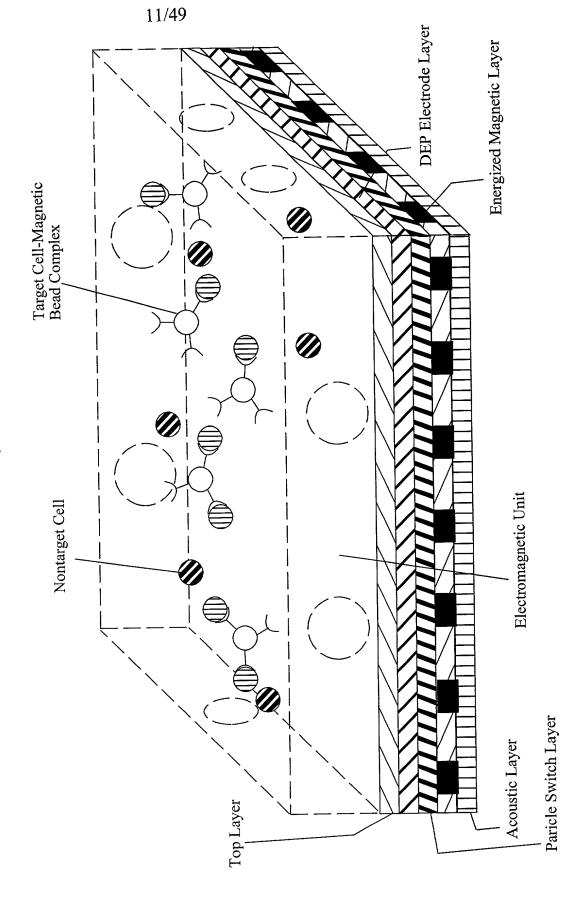
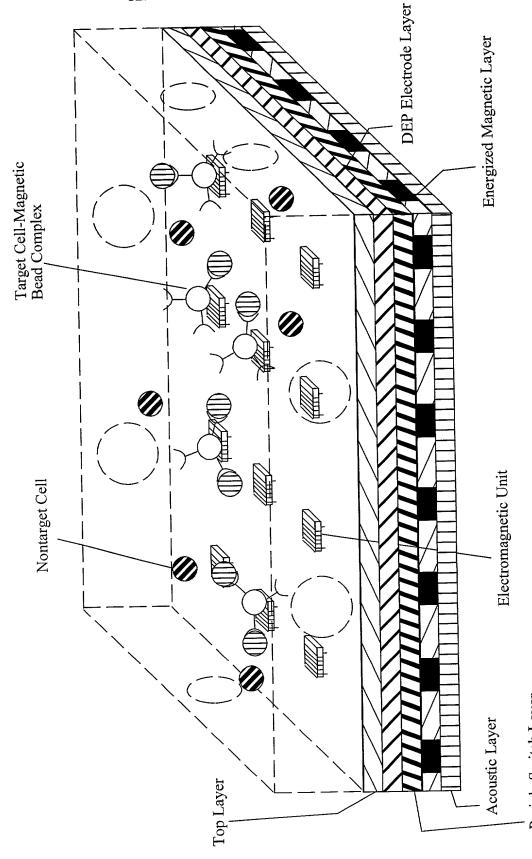


Figure 5B



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Paricle Switch Layer

Figure 5C

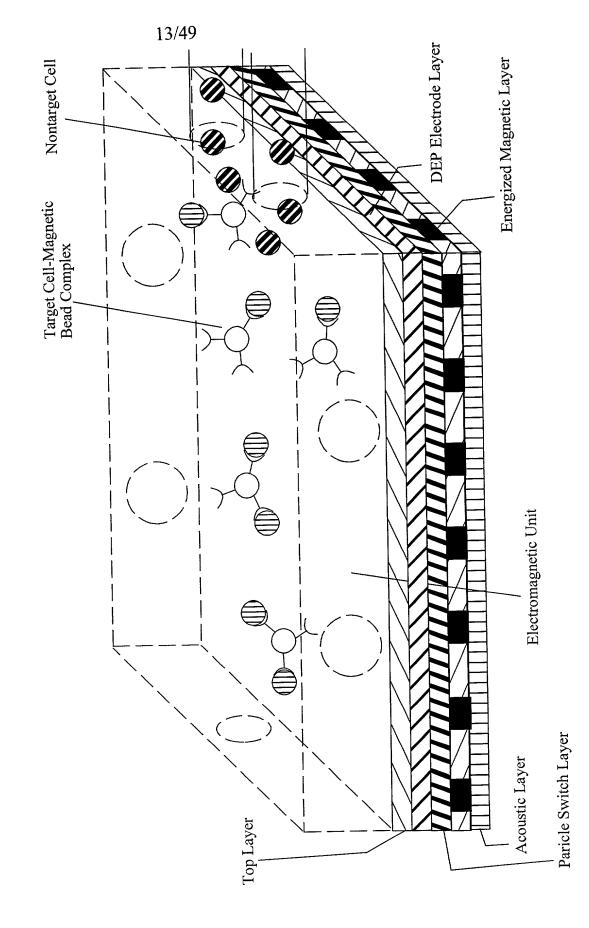


Figure 6

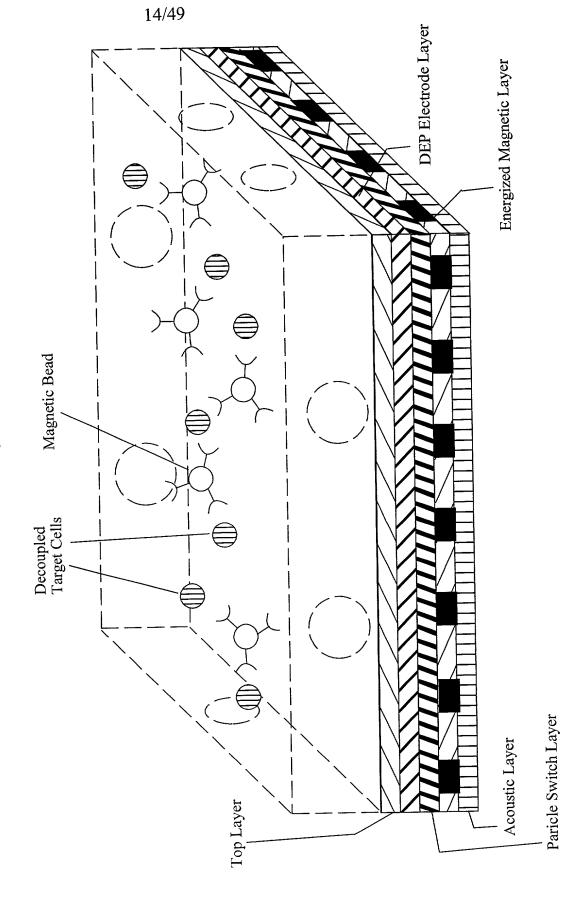
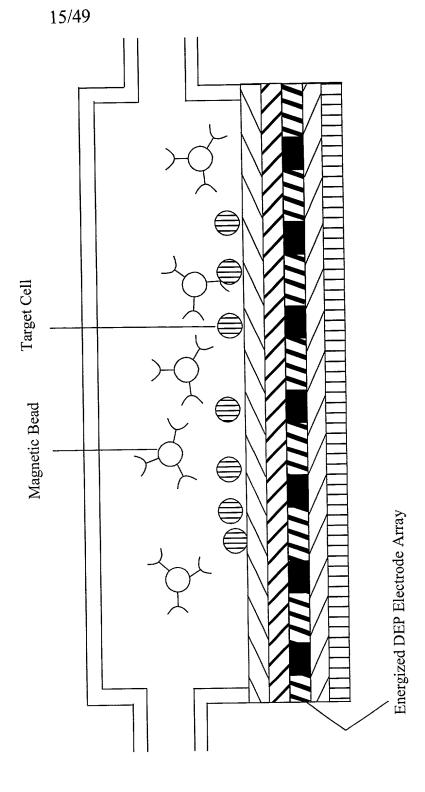


Figure 7A



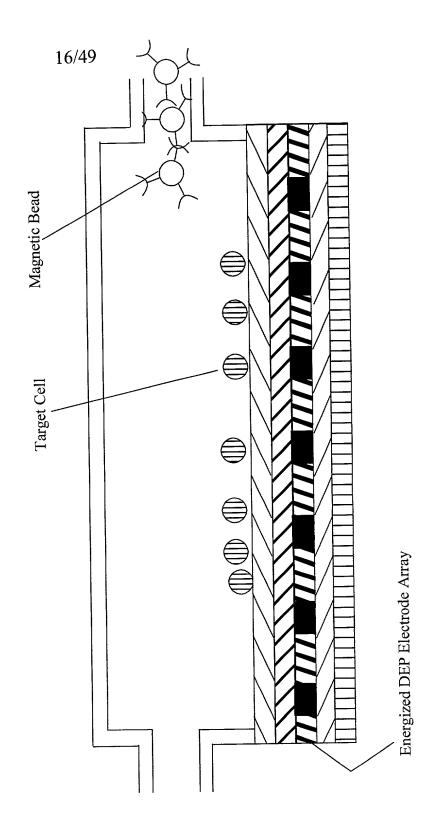


Figure 8

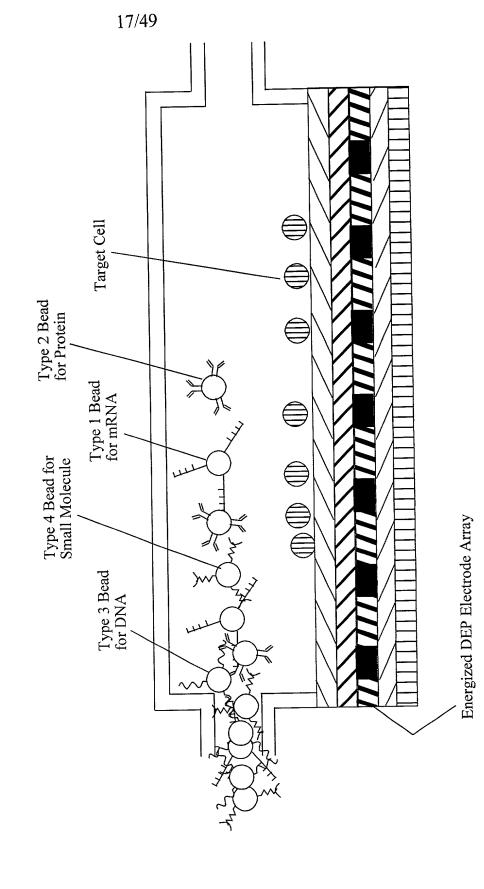


Figure 9A

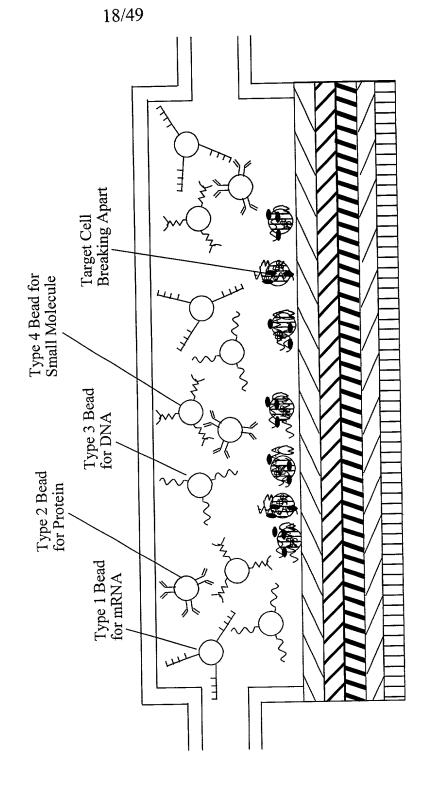


Figure 9B

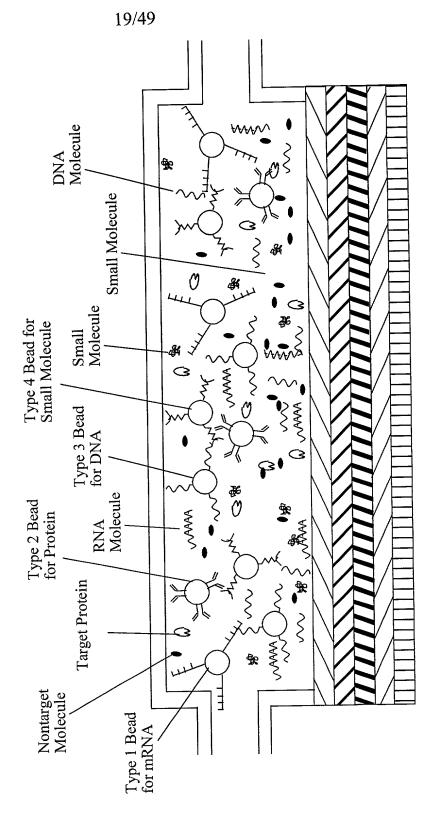


Figure 10

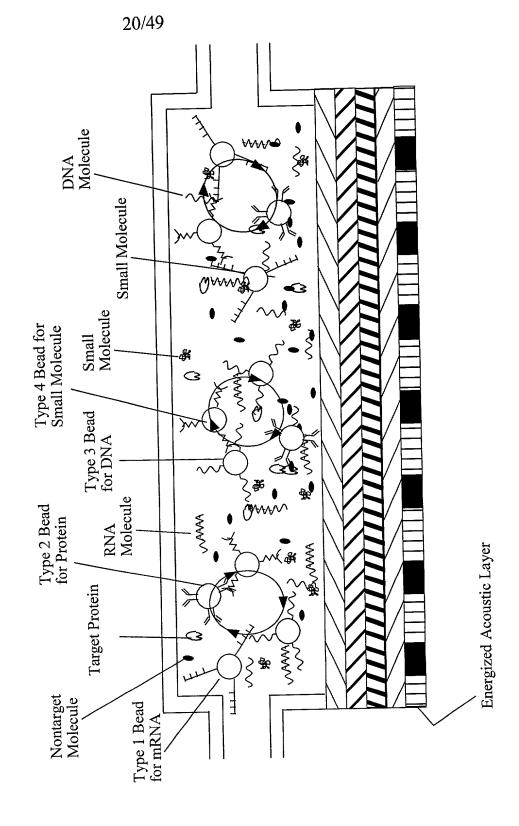


Figure 11

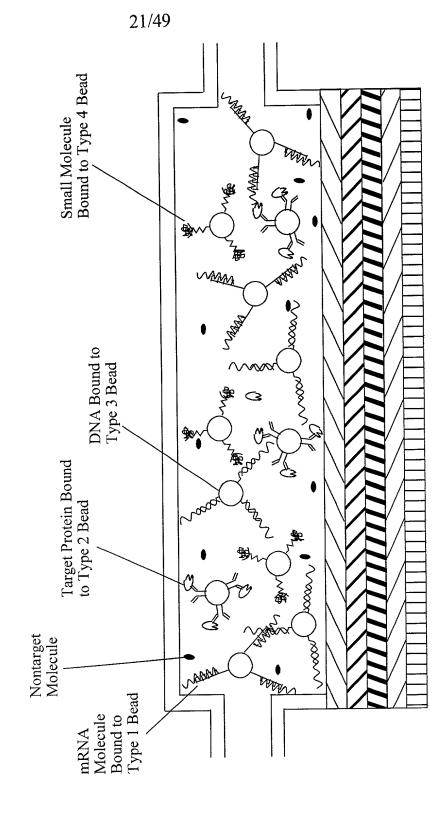


Figure 12A

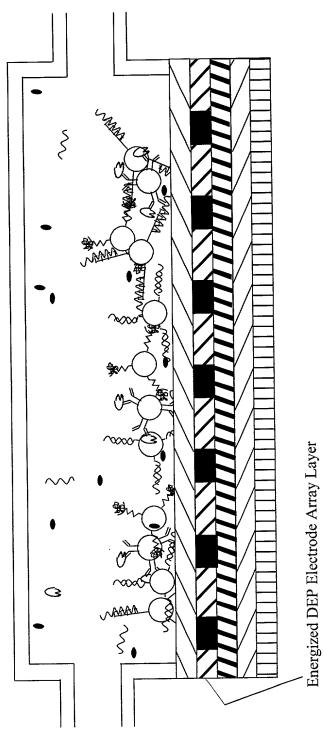
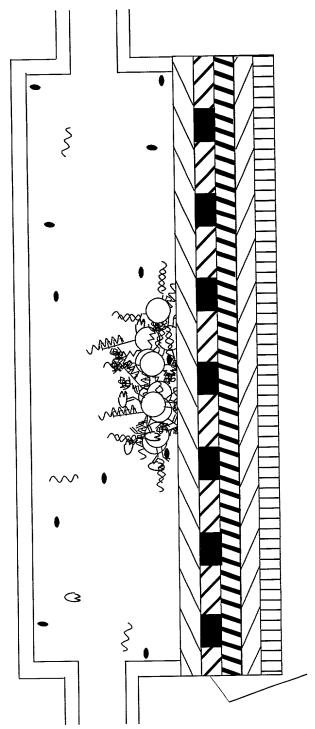


Figure 12B



Energized DEP Electrode Array Layer

Figure 13A

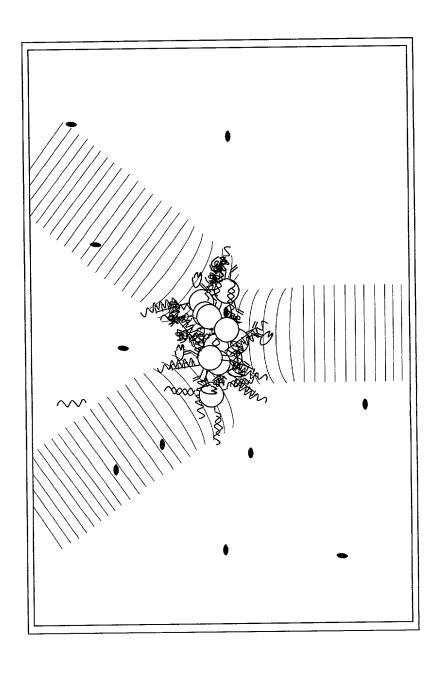
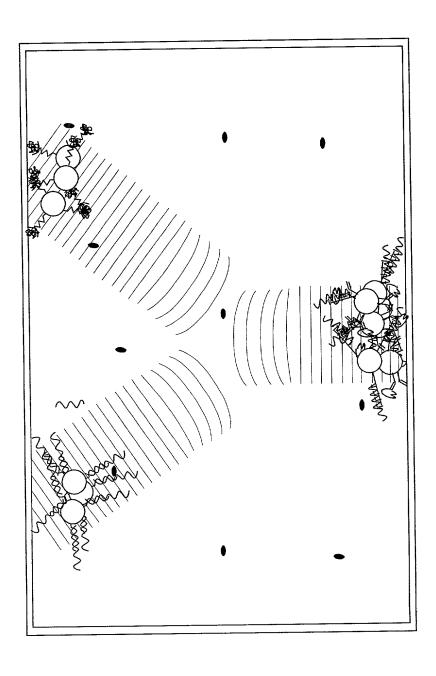


Figure 13B





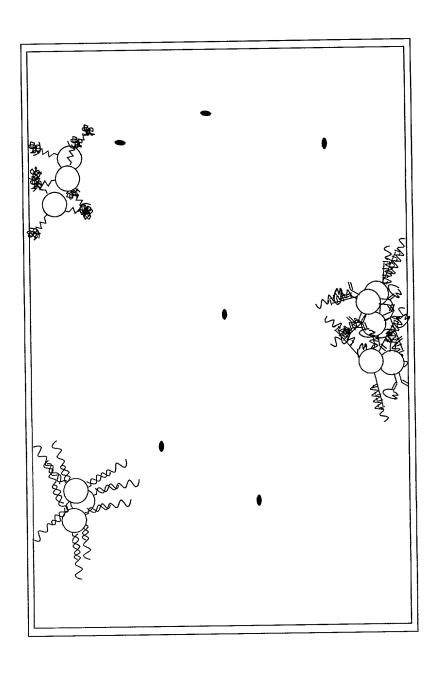


Figure 14A

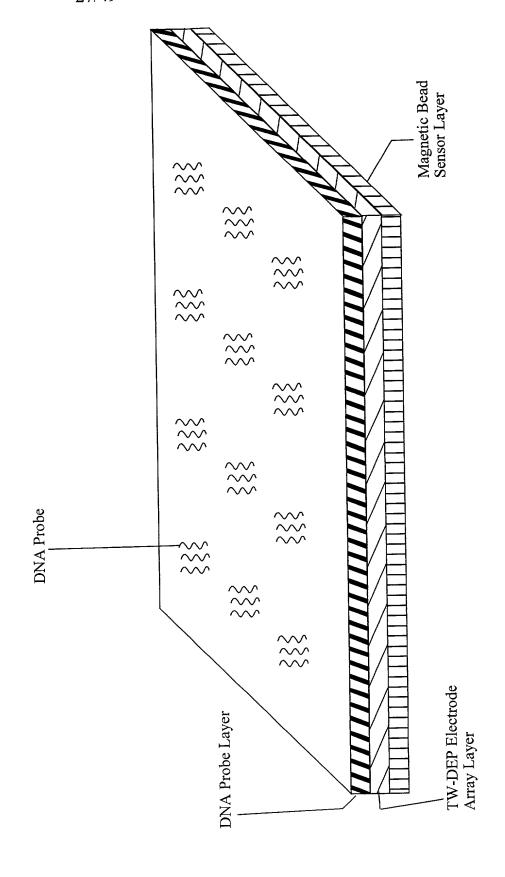


Figure 14B

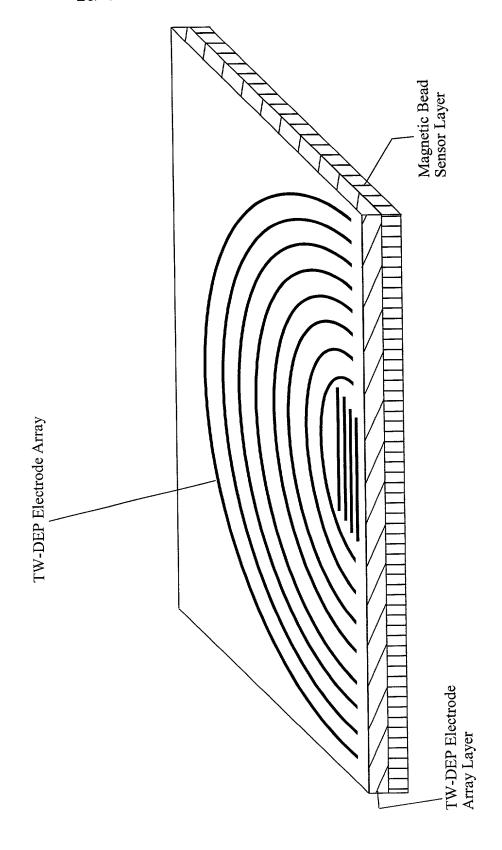


Figure 14C

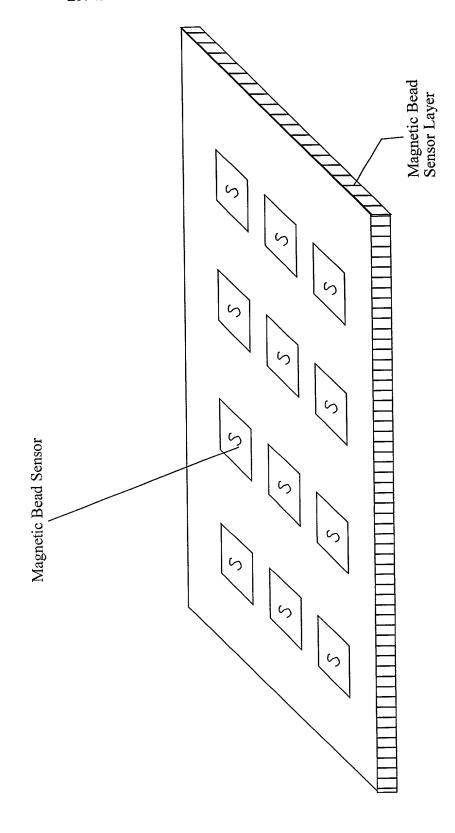


Figure 14D

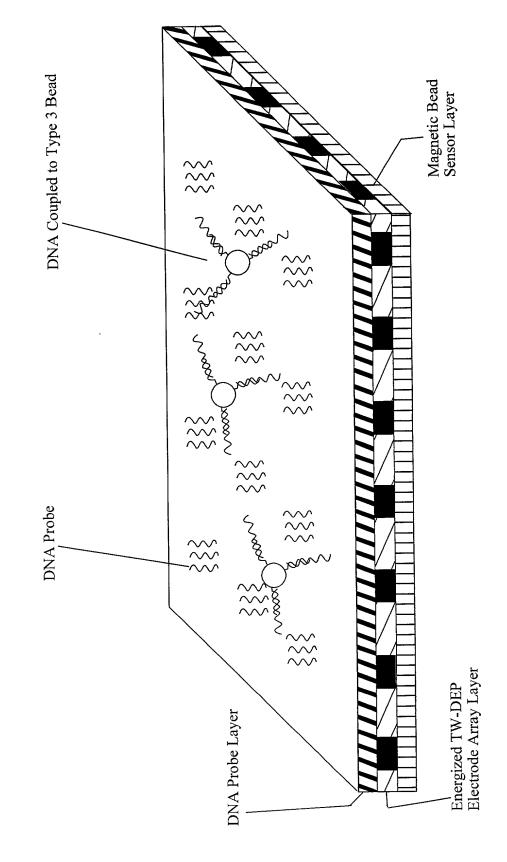


Figure 14E

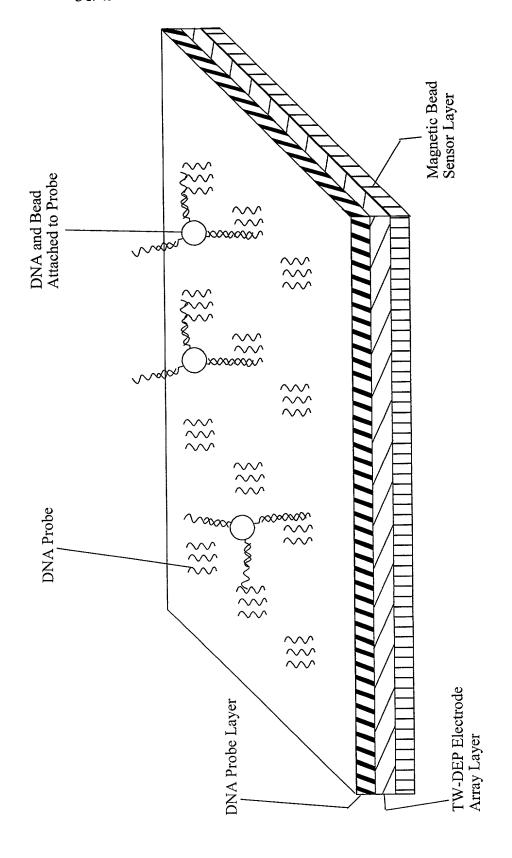


Figure 14F

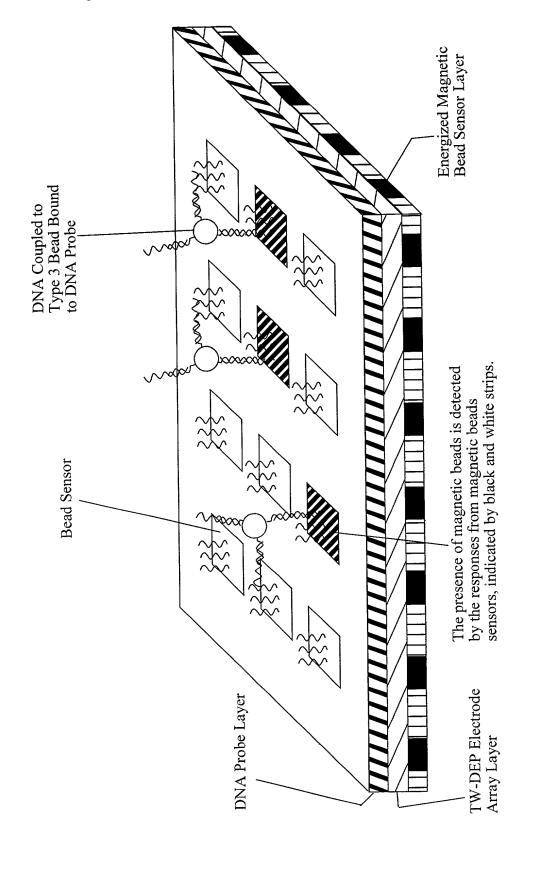


Figure 15A

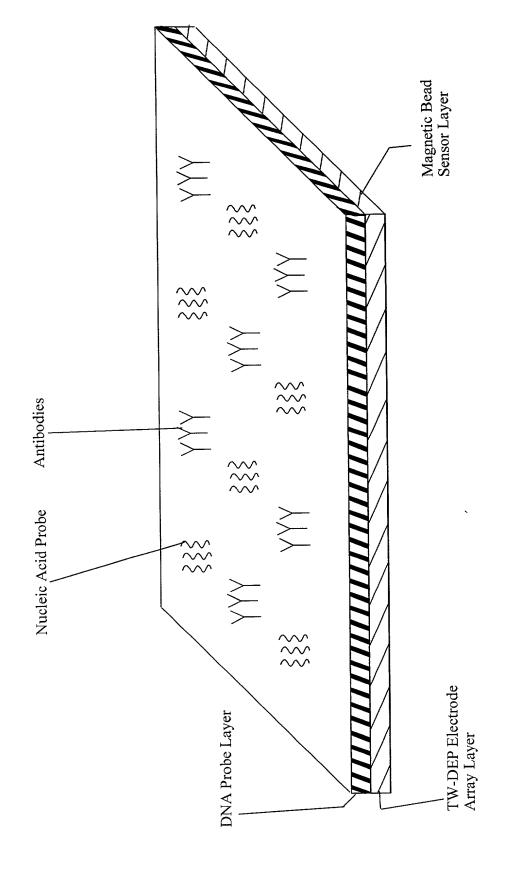


Figure 15B

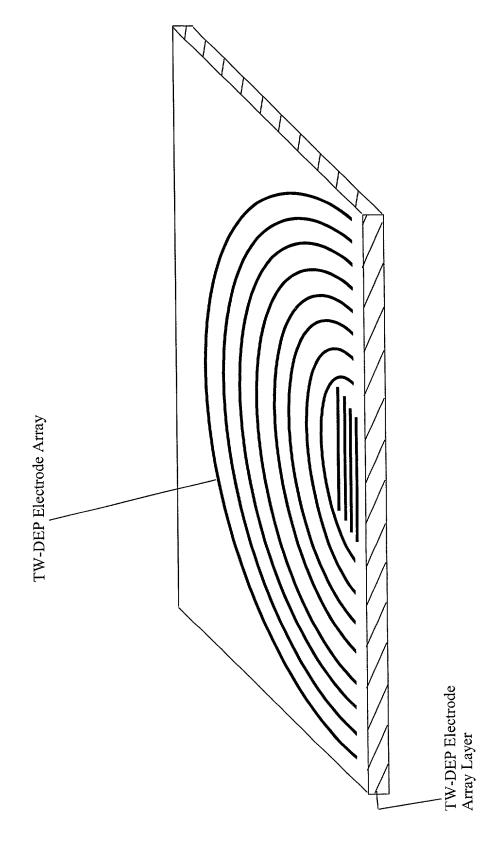
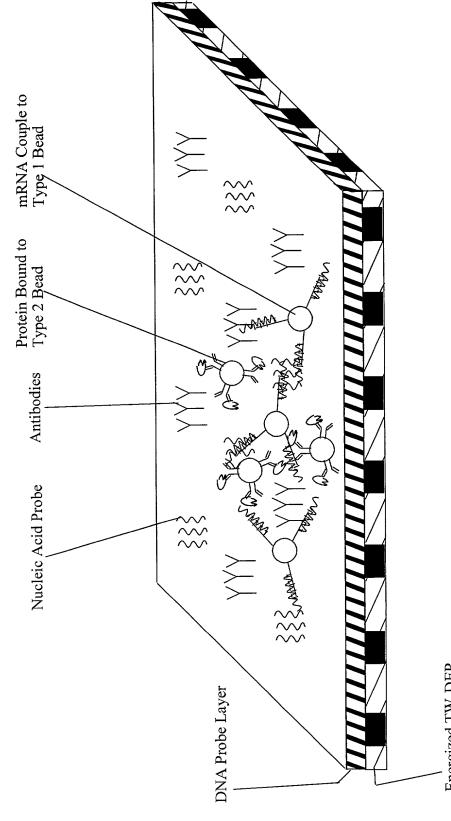


Figure 15C



Energized TW-DEP Electrode Array Layer

Figure 15D

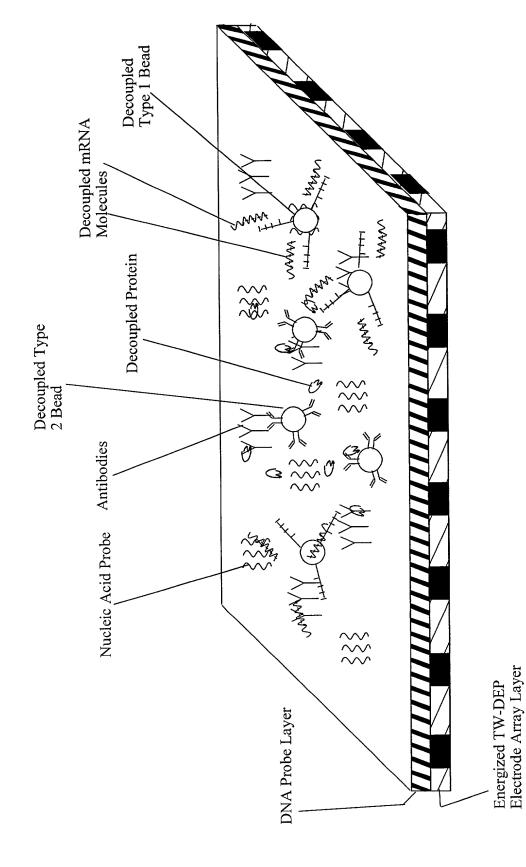


Figure 15E

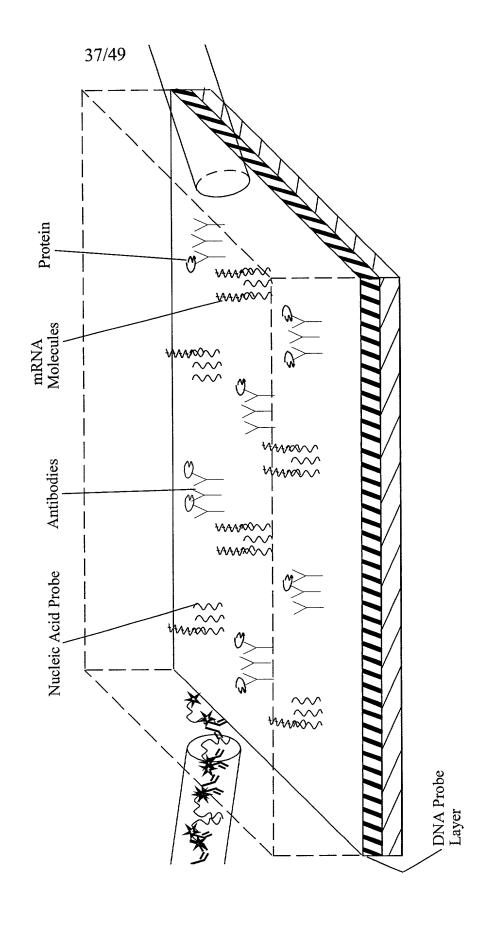


Figure 15F

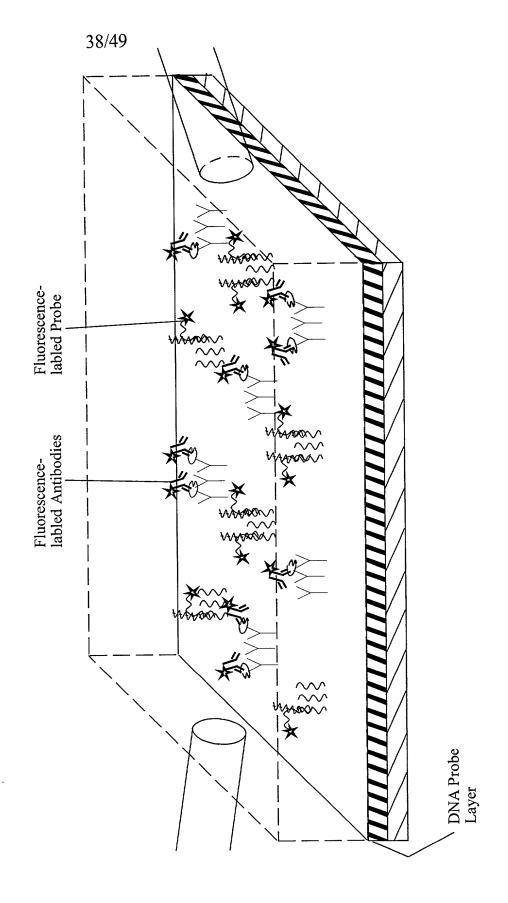


Figure 16A

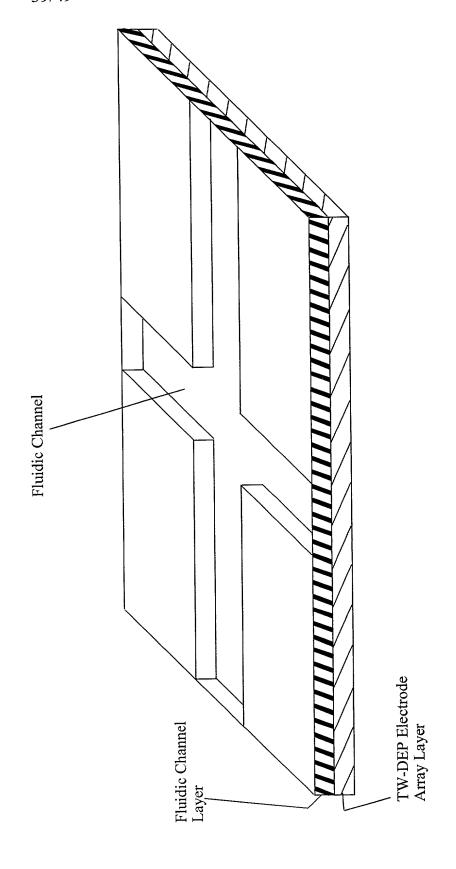


Figure 16B

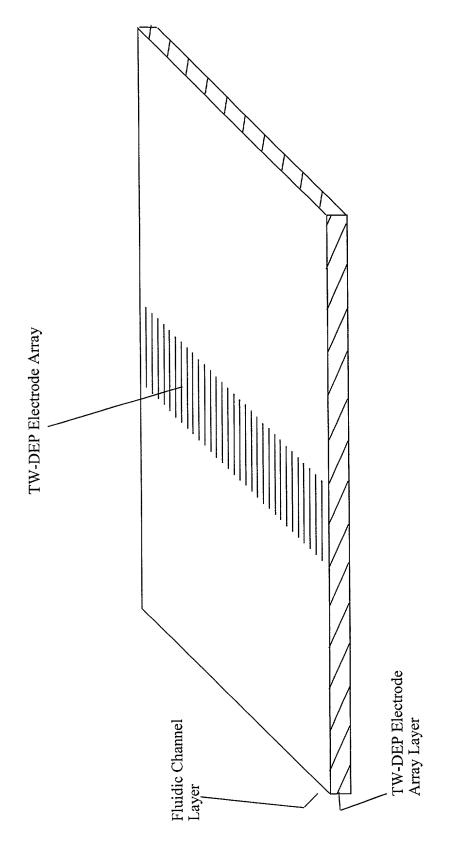


Figure 16C

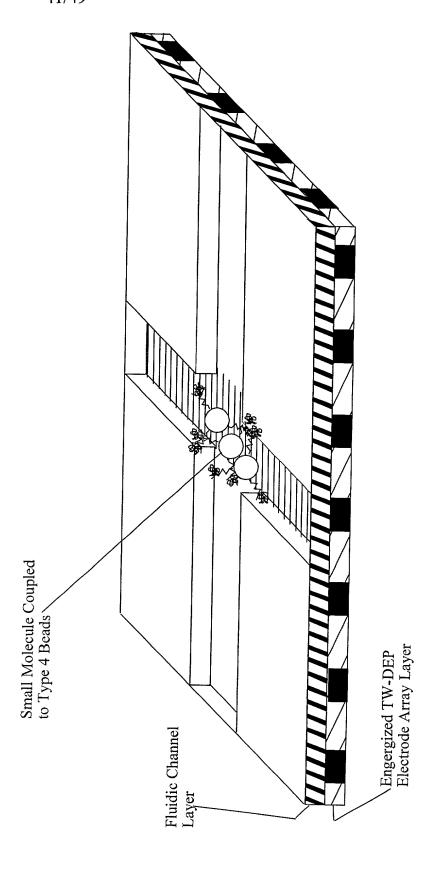


Figure 16D

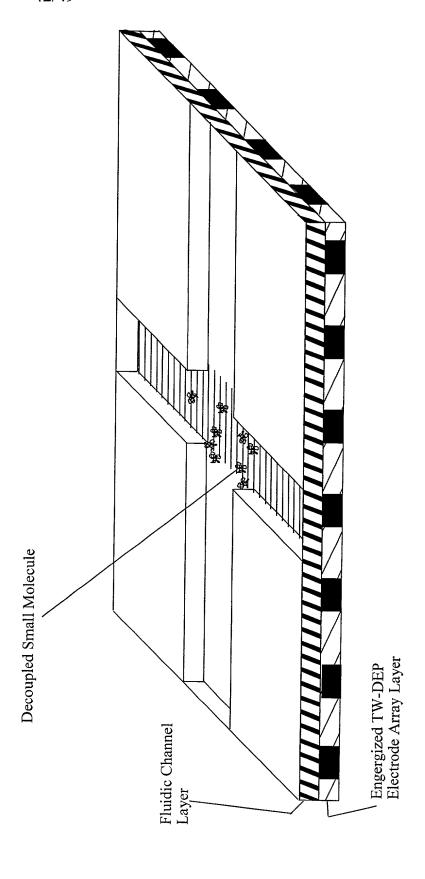


Figure 16E

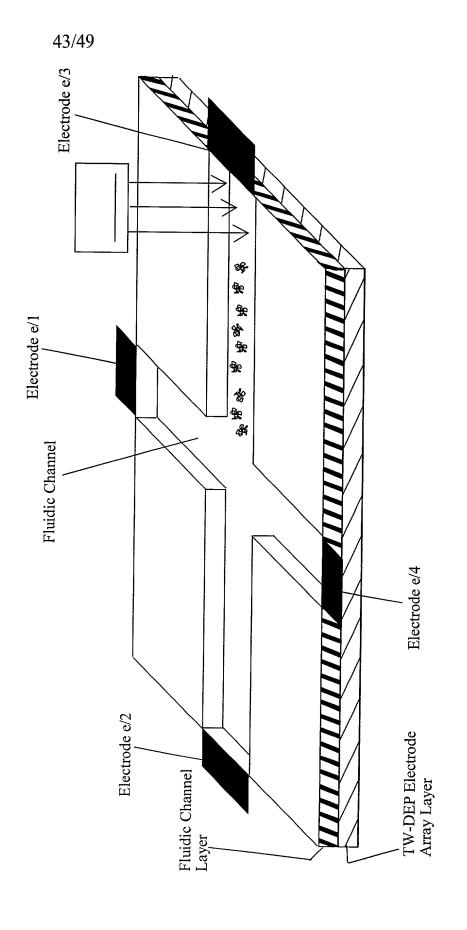
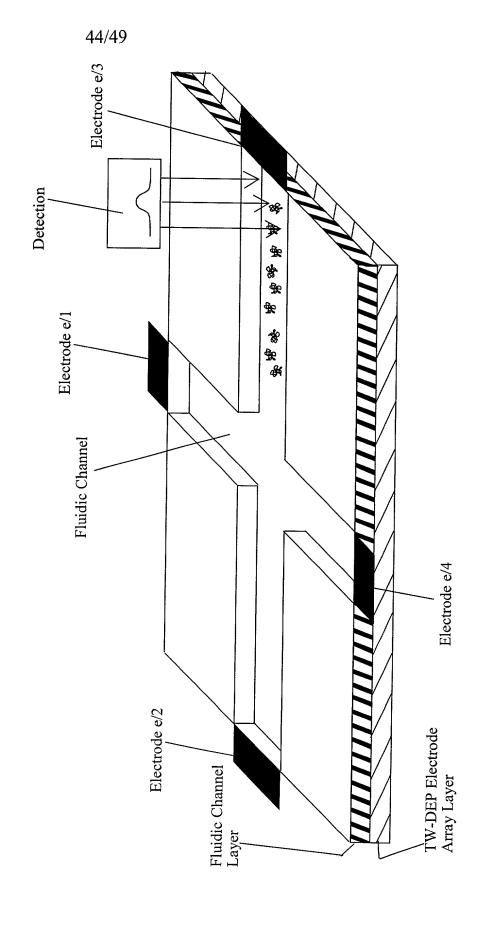
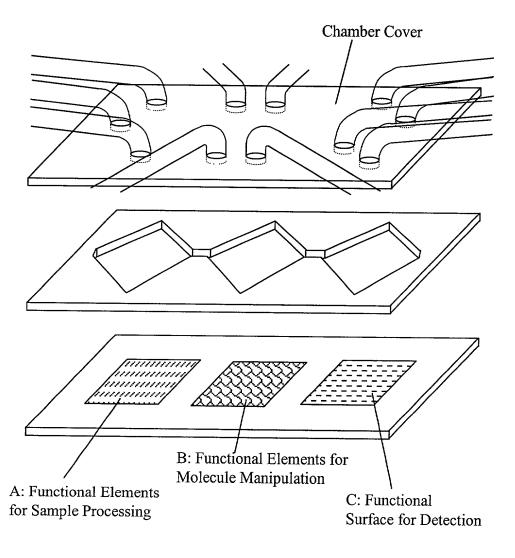


Figure 16F



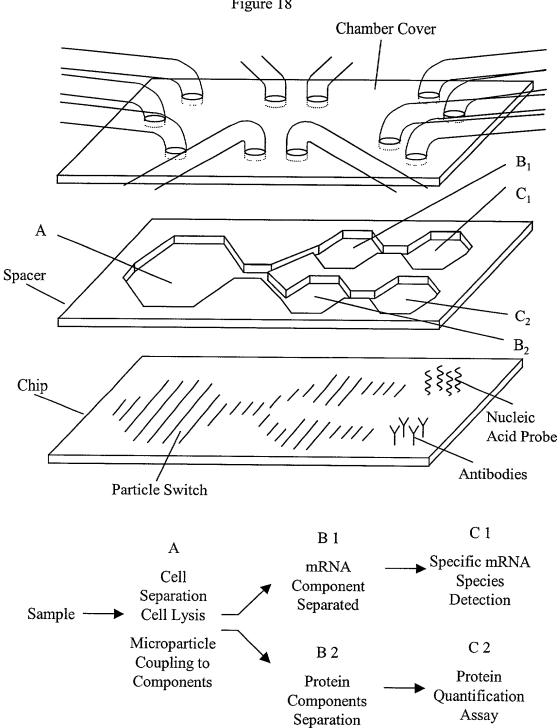
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## SINGLE CHIP SYSTEM



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Figure 18



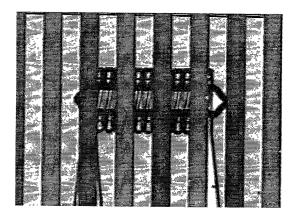


Figure 19A

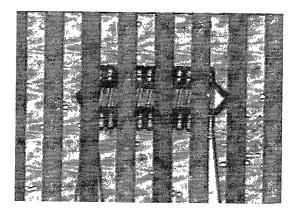


Figure 19B

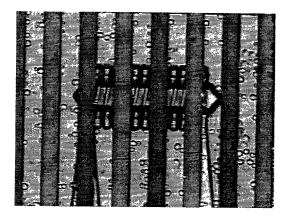


Figure 19C

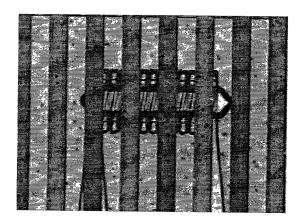


Figure 19D

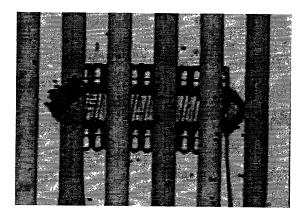
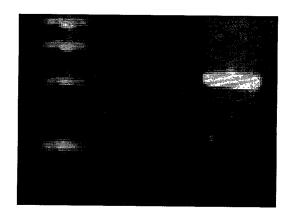


Figure 19E



Marker N-control G3PDH

Figure 19F